PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (Currently amended) A receiver unit, comprising:

a first buffer operative to receive and store digitized samples comprising multiple instances of a received signal; ~~and~~

a data processor coupled to the first buffer and operative to (a) retrieve different segments of the digitized samples one segment at a time from the first buffer, each of the retrieved segments comprising one of the multiple signal instances, ~~wherein the data processor is further operative to~~ (b) process two or more of the retrieved segments ~~at different times~~ one segment at a time with ~~the same corresponding segment of a~~ one programmed despreading sequence ~~programmed into the data processor~~ to provide ~~correlated~~ despread samples, (c) decover the despread samples with a channelization code of programmable length to provide decovered symbols, (d) demodulate the decovered symbols to provide demodulated symbols, and (e) combine the demodulated symbols from multiple signal instances to provide processed symbols;

a controller being operative to direct the data processor;

a microcontroller coupled to the data processor and the controller, the microcontroller being operative to receive tasks from the controller, instantiate a state machine for each task, and direct the data processor to process the retrieved multiple segments; and

an address generator coupled to the first buffer and the controller, the address generator being operative to implement a counter to control a write address for writing digitized samples to the first buffer, the counter being operative to send a signal to the controller to initiate processing of the stored samples by the data processor.

2. (Currently amended) The receiver unit of claim 1, ~~further comprising:~~

~~a controller coupled to the data processor and~~ wherein the controller is operative to dispatch tasks for the data processor and to process signaling data from the data processor.

3. (Canceled)

4. (Currently amended) The receiver unit of claim [[2]] 35, wherein the controller is operative to perform pilot processing and time tracking for each of the signal instances being processed.

5. (Currently amended) The receiver unit of claim [[2]] 35, wherein the controller is operative to perform lock detection for each of the signal instances being processed.

6. (Currently amended) The receiver unit of claim [[2]] 35, wherein the controller is operative to perform frequency tracking of the digitized samples.

7. (Currently amended) The receiver unit of claim [[1]] 35, further comprising:

a receiver operative to receive the multiple instances of the signal to provide the digitized samples.

8. (Currently amended) The receiver unit of claim [[1]] 35, wherein the data processor includes

a correlator operative to despread the retrieved segments of digitized samples with corresponding segments of PN (pseudo-random noise) despreading sequences to provide correlated samples~~, the correlated samples including the correlated samples from said two or more of the segments processed with the same segment of the despreading sequence~~.

9. (Currently amended) The receiver unit of claim 8, wherein the data processor further includes

a symbol ~~demodulation~~ demodulator and combiner coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols.

10. (Original) The receiver unit of claim 8, wherein the data processor further includes

an accumulator coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results.

11. (Original) The receiver unit of claim 9, wherein the data processor further includes

a second buffer coupled to the symbol demodulation and combiner and operative to store the processed symbols.

12. (Original) The receiver unit of claim 8, wherein the correlator includes

a set of K multipliers operative to concurrently despread sets of up to K complex digitized samples.

13. (Previously Presented) The receiver unit of claim 12, wherein the correlator further includes

a set of K summers coupled to the set of K multipliers, each summer operative to receive and sum pairs of samples from two of the multipliers.

14. (Previously Presented) The receiver unit of claim 8, wherein the correlator includes

an interpolator operative to receive and interpolate the despread samples to generate interpolated samples that are provided as the correlated samples.

15. (Currently amended) A receiver unit, comprising:

a first buffer operative to receive and store digitized samples at a particular sample rate; and

a data processor coupled to the first buffer and operative to retrieve segments of the digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate, and wherein the data processor includes a correlator operative to despread the retrieved segments of the digitized samples with corresponding segments of PN (pseudo-random noise) despreading sequences to provide correlated samples, the correlator including an interpolator operative to receive and interpolate the despread samples to generate interpolated samples that are provided as the correlated samples, and wherein the interpolator includes one or more pairs of scaling elements, each of the scaling elements operative to receive and scale respective despread samples with a particular gain to generate scaled samples, and one or more summer, each of the summers coupled to a respective pair of

scaling elements and operative to receive and sum the scaled samples from the pair of scaling elements to generate the interpolated samples.

16. (Currently amended) The receiver unit of claim 9, wherein the symbol ~~demodulation~~ demodulator and combiner includes

a decover element operative to receive and decover the correlated samples with one or more channelization codes to provide decovered symbols.

17. (Previously Presented) The receiver unit of claim 16, wherein the channelization codes are Walsh codes each having a length that is programmable and defined by one of the sets of the parameter values.

18. (Original) The receiver unit of claim 16, wherein the decover element is implemented with a fast Hadamard transform (FHT) element having L stages.

19. (Original) The receiver unit of claim 18, wherein the FHT element is operative to receive and process inphase and quadrature correlated samples on alternating clock cycles.

20. (Original) The receiver unit of claim 18, wherein the FHT element is operative to perform decovering with one or more Walsh symbols of a length of 1, 2, 4, 8, 16, 32, 64, or 128.

21. (Original) The receiver unit of claim 16, wherein the symbol demodulation and combiner further includes

a pilot demodulator coupled to the decover element and operative to demodulate the decovered symbols with pilot symbols to provide demodulated symbols.

22. (Currently amended) The receiver unit of claim 21, wherein the symbol ~~demodulation~~ demodulator and combiner further includes

a symbol accumulator coupled to the pilot ~~demodulation~~ demodulator and operative to accumulate the demodulated symbols from multiple signal instances to provide the processed symbols.

23. (Original) The receiver unit of claim 11, wherein the second buffer is operative to provide the processed symbols to a subsequent signal processing element in an output order that is different from an input order to provide de-interleaving of the processed symbols.

24. (Original) The receiver unit of claim 23, wherein the second buffer includes at least two sections, one section operative to store processed symbols for a current packet being processed and another section operative to store processed symbols for a prior processed packet to be provided to the subsequent signal processing element.

25. (Original) The receiver unit of claim 10, wherein the accumulator is operative to accumulate the correlated samples over a programmable time interval to provide pilot signal estimates.

26. (Currently amended) The receiver unit of claim 10, wherein the accumulator includes

a plurality of accumulate elements, each accumulate element operative to provide pilot signal estimate for ~~said different time offsets~~ a particular time offset.

27. (Currently amended) The receiver unit of claim [[2]] 35, wherein the controller is operative to instantiate a timing state machine for each signal instance being processed.

28. (Original) The receiver unit of claim 27, wherein each instantiated timing state machine includes

a time tracking loop operative to track movement of the signal instance being processed.

29. (Currently amended) The receiver unit of claim [[2]] 35, wherein the controller is operative to receive a timing signal and initiate processing of the segments of digitized samples in response to the received timing signal.

30. (Original) The receiver unit of claim 29, wherein the timing signal is generated based on a comparison value provided by the controller.

31. (Original) The receiver unit of claim 29, wherein the timing signal is indicative of a particular number of digitized samples having been stored to the first buffer.

32. (Currently amended) The receiver unit of claim [[2]] 35, wherein the ~~digital samples are sampled at a sample rate, and wherein the data processor is operated with a~~ processing clock ~~having~~ has a frequency that is at least ten times higher than the sample rate, the sample rate being asynchronous with the processing clock[[,]].

33. (Currently amended) The receiver unit of claim [[2]] 1, ~~further comprising~~ [[a]] wherein the micro-controller ~~coupled to the controller and~~ is operative to receive the ~~dispatched~~ tasks and [[to]] generate a set of control signals to direct the operation of the first buffer and the data processor to execute the dispatched tasks.

34. (Currently amended) The receiver unit of claim [[33]] 35, wherein the micro-controller is operative to instantiate a task state machine for each task being processed.

35. (Currently amended) A receiver unit, in a wireless communications system, comprising:

a first buffer operative to receive and store digitized samples at a particular sample rate;

a data processor coupled to the first buffer and operative to retrieve segments of the digitized samples from the first buffer and to process each of the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate;

a controller coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor; and

a micro-controller coupled to the controller and operative to receive the dispatched tasks and to generate a set of control signals to direct the operation of the first buffer and the data processor to execute the dispatched tasks, wherein the micro-controller includes a set of latches operative to latch a dispatched task and one or more parameter values to be applied for the dispatched task, at least one counter, each of the counters coupled to a respective latch and operative to provide an indicator signal based on a value stored in the latch, and a sequencing controller operative to receive at least one indicator signal and the dispatched task and to generate the set of control signals.

36. (Currently amended) The receiver unit of claim [[1]] 35, further comprising:

a data interface coupled to the first buffer, the data interface operative to receive the digitized samples, discard unnecessary samples, and assemble the samples into words suitable for efficient storage to the first buffer.

37. (Currently amended) The receiver unit of claim [[1]] 35, wherein a word of 32 bits or more is written to the first buffer or read from the first buffer for each buffer access.

38. (Currently amended) The receiver unit of claim [[1]] 35, wherein the first buffer is operative to store two or more packets of digitized samples.

39. (Currently amended) The receiver unit of claim [[1]] 35, wherein the ~~digitized samples received and stored in the~~ first buffer ~~comprises~~ is further operative to store pseudo-random noise (PN) samples.

40-42. (Cancelled)

43. (Currently amended) The receiver unit of claim 1, wherein the ~~digital samples are sampled at a sample rate, and wherein the data processor is operated with a processing~~ clock ~~having a~~ frequency of the data processor ~~that~~ is at least ten times higher than the sample rate.

44. (Previously Presented) The receiver unit of claim 1, wherein the receiver unit is configured for operation in a high data rate (HDR) CDMA system.

45-47. (Cancelled)

48. (Currently amended) A method for processing a received signal in a wireless communications system, the method comprising:

~~receiving, processing, and digitizing multiple signal instances of a transmitted signal to provide digitized samples;~~

buffering ~~the~~ digitized samples of a received signal in a first buffer;

retrieving ~~different~~ segments of the digitized samples from the first buffer~~, each of the retrieved segments having one of the signal instances~~; ~~and~~

processing ~~two or more~~ each of the retrieved segments ~~at different times with a data processor programmed with the same corresponding segment of a despreading sequence to provide correlated samples~~ with a particular set of parameter values;

dispatching tasks for a data processor to process the retrieved segments and to process signaling data from the data processor;

receiving the dispatched tasks and generating a set of control signals to direct the operation of the first buffer and the data processor to execute the dispatched tasks;

latching a dispatched task and one or more parameter values to be applied for the dispatched task;

providing an indicator signal based on a value stored in the latch; and

receiving at least one indicator signal and the dispatched task and to generate the set of control signals.

49. (Currently amended) The method of claim 48, wherein the processing of the ~~signal instances~~ segments includes despreading the retrieved segments of digitized samples with corresponding segments of PN (pseudo-random noise) despreading sequences to provide correlated samples~~, the correlated samples including the correlated samples from said two or more of the segments processed with the same segment of the despreading sequence~~.

50. (Original) The method of claim 49, wherein the processing further includes decovering the correlated samples with one or more channelization codes to provide decovered symbols.

51. (Original) The method of claim 50, wherein the processing further includes demodulating the decovered symbols with pilot symbols to provide demodulated symbols.

52. (Original) The method of claim 51, wherein the processing further includes accumulating the demodulated symbols from multiple signal instances to provide processed symbols.

53. (Currently amended) The method of claim 48, wherein the digital samples are received, processed and digitized at a sample rate, and wherein the ~~signal instances~~ retrieved segments are processed by the data processor with a processing clock having a frequency that is higher than the sample rate, the sample rate being asynchronous with the processing clock, the method further comprising:

tracking a chip rate of the digitized samples; and

providing a signal used to write digitized samples to the first buffer starting at designated locations.

54. (Currently amended) The method of claim 48 wherein the processing of the signal instances ~~includes~~ comprises:

despreading the retrieved segments of the digitized samples with corresponding segments of PN (pseudo-random noise) despreading sequences to provide correlated samples~~, the correlated samples including the correlated samples from said two or more of the segments processed with the same segment of the despreading sequence,~~;

decovering the correlated samples with one or more channelization codes to provide decovered symbols[[,]];

demodulating the decovered symbols with pilot symbols to provide demodulated symbols[[,]]; and

accumulating the demodulated symbols from the multiple signal instances to provide processed symbols.

55-56. (Cancelled)

57. (Currently amended) The receiver unit of claim 1 ~~further comprising a~~ wherein the controller ~~having~~ has a time tracking loop operative to track movement of one of the signal instances being processed by the data processor, and further being configured to generate ~~the~~ a time offset used to retrieve a segment of the digitized samples in the first buffer containing said one of the signal instances in response to the time tracking loop.

58. (Previously Presented) The receiver unit of claim 1 wherein the data processor is further configured to coherently combine the correlated samples from said two or more of the segments to generate processed symbols.

59. (canceled)

60. (New) The receiver unit of claim 35, wherein at least one of the parameter values is programmable.

61. (New) A method comprising:

storing digitized samples comprising multiple instances of a received signal at a first buffer;

at a data processor, retrieving different segments of the digitized samples one segment at a time from the first buffer, each of the retrieved segments comprising one of the multiple signal instances;

process two or more of the retrieved segments one segment at a time with one programmed despreading sequence to provide despread samples;

decovering the despread samples with a channelization code of programmable length to provide decovered symbols;

demodulating the decovered symbols to provide demodulated symbols;

combining the demodulated symbols from multiple signal instances to provide processed symbols;

receiving tasks, instantiating a state machine for each task, and directing the data processor to process the retrieved multiple segments;

implementing a counter to control a write address for writing digitized samples to the first buffer; and

sending a signal to the controller to initiate processing of the stored samples by the data processor.